N.D. Mehta, Assistant Professor, VGEC Chandkheda

**Switching waveforms of a transistor:**

A transistor cannot be turned on instantaneously because of presence of internal capacitances. The figure 1 shows the switching waveforms of an NPN transistor with resistive load between collector and emitter.

When base-emitter voltage is $V_{BE}$ is applied, the base current rises to $I_{BS}$. The collector current however remains zero or equal to collector-emitter leakage current $I_{CE0}$ as shown in figure. 1.

After some time delay $t_d$ called delay time, the collector current begins to rise. This delay is due to the time required to charge base emitter capacitance to VBES=0.7V.
After this delay $t_d$, Collector current rises to steady state value $I_{CS}$ in time $t_r$, which is known as "Rise Time". This means that turn on time for BJT is $t_{on} = t_d + t_r$ .

Rise time depends upon the input capacitance. During rise time $t_r$, Collector-emitter voltage falls from $V_{CC}$ to $V_{CES}$. When the base-emitter voltage $V_{BE}$ is removed at time t1, the collector current doesn't change for a time ts, called "Storage time".
During ts, saturating charge is removed from the base. After $t_s$, collector current begins to fall and at the same time collector voltage starts building up. After time $t_f$ , called "Fall Time". $I_C$ decreases to $I_{CE0}$ (Almost zero) and collector-emitter voltage rises to $V_{CC}$. Sum of "Storage time" and "fall time" gives "Turn off" time.

(ie) $t_{off} = t_s + t_f$

The various waveforms during the transistor switching are shown in figure.
$t_{on}$ - On time $t_{off}$ – Off time $t_s$ - Storage time $t_d$ - Delay time $t_f$ - Fall time $t_n$ - Conduction time

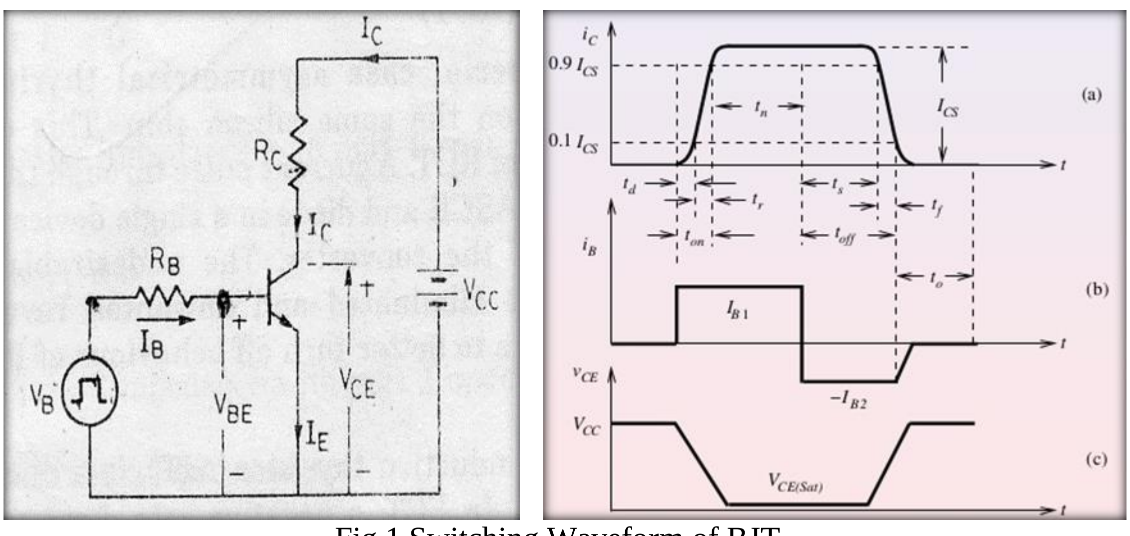

Fig.1 Switching Waveform of BJT

Following are the important points about BJT to be remembered when designing the base drive circuit for the transistor.

1. BJT is a current controlled device. Its operation is controlled by the base current.
2. The Power BJT is used as ON/OFF switch in the power converter circuits.

N.D. Mehta, Assistant Professor, VGEC Chandkheda

3. Power BJT operates in saturation and cutoff region when used as a switch. ie, when the device operates in saturation region it is in ON and when the device operates in cutoff region, it is in OFF state.
4. Sufficient base current is required to drive BJT in saturation.
5. Amount of carrier injected in base region determine storage time of BJT.
6. Storage time determines turn-on and turn-off times of the transistor.
7. There should be mechanism to control the amount of saturation so as to control storage time.

**Baker's Clamp Circuit:**

Baker clamp is a generic name for a class of electronic circuits that reduce the storage time of a switching bipolar junction transistor (BJT) by applying a nonlinear negative feedback through various kinds of diodes. The reason for slow turn-off times of saturated BJTs is the stored charge in the base. It must be removed before the transistor will turn off since the storage time is a limiting factor of using bipolar transistors and IGBTs in fast switching applications. The diode-based Baker clamps prevent the transistor from saturating and thereby accumulating a lot of stored charge.

The Baker clamp introduces a nonlinear negative feedback into a common-emitter stage (BJT switch), with the purpose to avoid saturation by decreasing the gain near the saturation point. While the transistor is in active mode and it is far away enough from the saturation point, the negative feedback is turned off and the gain is maximal; when the transistor approaches the saturation point, the negative feedback gradually turns on, and the gain quickly drops. To decrease the gain, the transistor acts as a shunt regulator with regard to its own base–emitter junction: it diverts a part of the base current to ground by connecting a voltage-stable element in parallel to the base–emitter junction.

A combination of large reverse base drive and anti-saturation techniques may be used to reduce storage time to almost zero. A circuit baker's clamp may be employed as illustrated in Fig.2

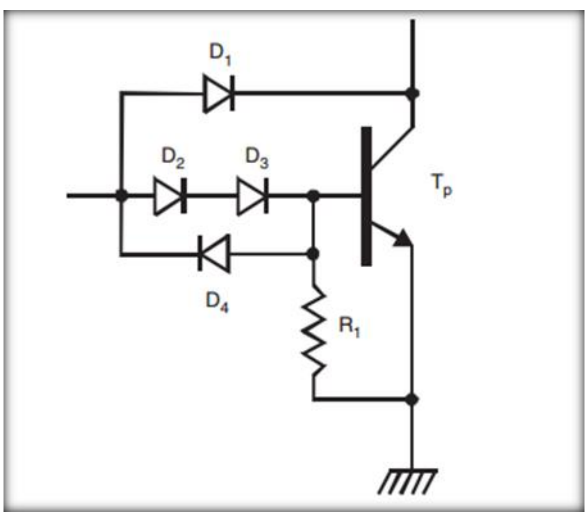


Fig. 2 Baker Clamp Circuit

N.D. Mehta, Assistant Professor, VGEC Chandkheda

When the transistor is on, its base is two diode drops below the input. Assume that diodes $D_2$ and $D_3$ have a forward-bias voltage of about 0.7V, and then the base will be 1.4V below the input terminal. Due to diode $D_1$ the collector is one diode drop or 0.7V below the input. Therefore, the collector will always be more positive than the base by 0.7V, staying out of saturation and because collector increases, the gain β also increases a little bit. Diode $D_4$ provides a negative path for the reverse base current.

The most interesting results occur with a fixed base drive and a variable collector current, a common situation in a switching power supply. The effect upon storage time is shown in Figure 3. Note that use of the Baker Clamp has achieved a remarkable reduction in storage time at low collector currents and its value is somewhat independent of collector current. Improvement in fall time is even more spectacular as shown in Figure 3. The trade-off made for the improved switching performance is an increased on-state voltage. It is typically 0.3 V in hard saturation and 0.9 V with the Baker clamp.

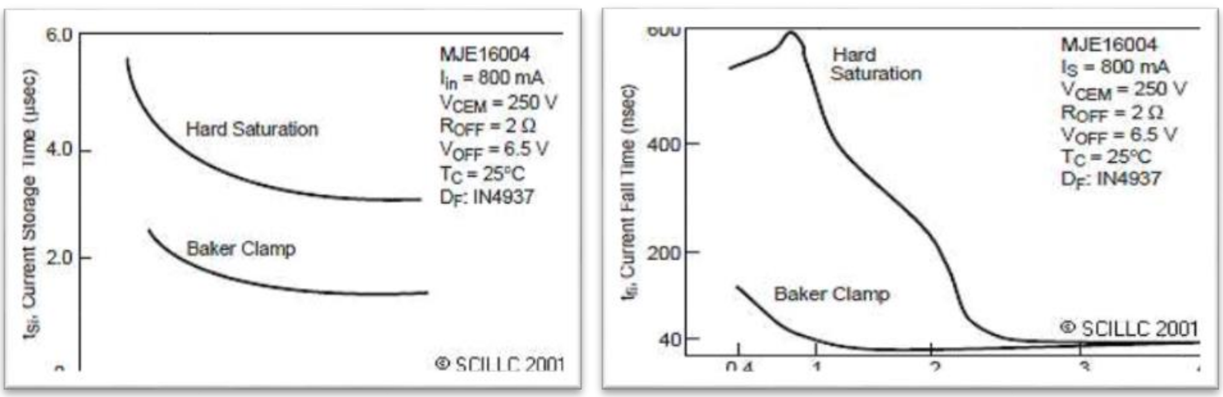


Fig. 3 Storage Time with Fixed Drive in a Baker Clamp Circuit & Fall Time with Fixed Drive in a Baker Clamp Circuit